What is claimed is:

[Claim 1] 1. A field effect transistor, comprising:

a gate electrode formed on a top surface of a gate dielectric layer, said gate dielectric layer on a top surface of a single-crystal silicon channel region, said single-crystal silicon channel region on a top surface of a Ge comprising layer, said Ge comprising layer on a top surface of a single-crystal silicon substrate, said Ge comprising layer between a first dielectric layer and a second dielectric layer on said top surface of said single-crystal silicon substrate.

[Claim 2] 2. The field effect transistor of claim 1, wherein said first dielectric layer extends under a first side of said gate electrode and said second dielectric layer extends under a second and opposite side of said gate electrode.

[Claim 3] 3. The field effect transistor of claim 1, wherein said first dielectric layer extends under a first side of said single-crystal silicon channel region and said second dielectric layer extends under a second and opposite side of said single-crystal silicon channel region.

[Claim 4] 4. The field effect transistor of claim 1, further including:

a polysilicon source region and a polysilicon drain region, each abutting said single-crystal silicon channel region on opposite sides of said single-crystal silicon channel region.

[Claim 5] 5. The field effect transistor of claim 4, wherein said first dielectric layer extends under said polysilicon source and said second dielectric layer extends under said polysilicon drain.

[Claim 6] 6. The field effect transistor of claim 4, wherein said first dielectric layer does not extend under said polysilicon source and said second dielectric layer does not extend under said polysilicon drain.

[Claim 7] 7. The field effect transistor of claim 5, wherein:

a first region of said first dielectric layer under said single-crystal silicon channel region has a first thickness and a second region of said first dielectric layer under said polysilicon source region has a second thickness, said first thickness greater than said second thickness; and
a first region of said second dielectric layer under said single-crystal silicon channel region has a first thickness and a second region of said second dielectric layer under said polysilicon drain region has a second thickness, said first thickness greater than said second thickness.

[Claim 8] 8. The field effect transistor of claim 4, further including:

a single-crystal silicon source region between said polysilicon source region and said single-crystal silicon channel region; and
a single-crystal silicon source drain between said polysilicon drain region and said single-crystal silicon channel region.

[Claim 9] 9. The field effect transistor of claim 8, wherein said single-crystal silicon source region and said single-crystal silicon drain region each extend under said gate electrode.

[Claim 10] 10. The field effect transistor of claim 8, wherein:

a first region of said first dielectric layer under said single-crystal silicon channel region has a first thickness and a second region of said first dielectric layer under said polysilicon source region has a second thickness, said first thickness greater than said second thickness;

a first region of said second dielectric layer under said single-crystal silicon channel region has a first thickness and a second region of said second dielectric layer under said polysilicon drain region has a second thickness, said first thickness greater than said second thickness;

said single-crystal silicon source region extends into said polysilicon source region past said first region of said first dielectric layer; and

said single-crystal silicon drain region extends into said polysilicon drain region past said first region of said second dielectric layer.

[Claim 11] 11. The field effect transistor of claim 10, wherein:

said single-crystal silicon source region does not extend into said single-crystal silicon channel region past said first region of said first dielectric layer; and

said single-crystal silicon drain region does not extend into said single-crystal silicon channel region past said first region of said second dielectric layer.

[Claim 12] 12. The field effect transistor of claim 1, wherein bottom surfaces of said first and second dielectric layers extend into said single-crystal silicon substrate past a bottom surface of said Ge comprising layer.

[Claim 13] 13. The field effect transistor of claim 1, wherein said Ge comprising layer comprises $Si_{(1-X)}Ge_X$ where X equals about 0.15 to about 0.5 or $Si_{(1-X-Y)}Ge_XC_Y$ where X equals about 0.15 to about 0.5 and Y equals about 0 to about 0.1.

[Claim 14] 14. The field effect transistor of claim 1, wherein said first and second dielectric layers induce stress in the crystal lattice of said channel region.

[Claim 15] 15. The field effect transistor of claim 1, wherein said first dielectric layer and second dielectric layer each comprise oxides of silicon and oxides of germanium.

[Claim 16] 16. The field effect transistor of claim 1, further including:

a P doped polysilicon source region and a P-doped polysilicon drain region, each abutting said single-crystal silicon channel region on opposite sides of said single-crystal silicon channel region; and

a dielectric isolation abutting said polysilicon source and said polysilicon drain, said first and second dielectric layers extending, respectively, under said polysilicon source and said polysilicon drain and abutting said dielectric isolation.

[Claim 17] 17. The field effect transistor of claim 1, further including:

an N doped polysilicon source region and an N-doped polysilicon drain region, each abutting said single-crystal silicon channel region on opposite sides of said single-crystal silicon channel region; and

a dielectric isolation abutting said polysilicon source and said polysilicon drain.

[Claim 18] 18. The field effect transistor of claim 1, wherein said single-crystal silicon channel region is doped N-type.

[Claim 19] 19. The field effect transistor of claim 1, wherein said single-crystal silicon channel region is doped P-type.

[Claim 20] 20. A method of fabricating a field effect transistor, comprising:

(a) providing a single-crystal silicon substrate having a single-crystal Ge comprising layer formed on a top surface of said single-crystal silicon substrate and a single-crystal silicon layer formed on a top surface of said single-crystal Ge comprising layer;

(b) forming a gate dielectric layer on a top surface of said single-crystal silicon layer;

(c) forming a gate electrode on a top surface of said dielectric layer;

(d) removing said single-crystal silicon layer to form a single crystal-silicon island and removing a less than whole portion of said single-crystal Ge comprising layer to form an island of single-crystal silicon under said gate electrode where said single-crystal silicon layer and said single-crystal Ge comprising layer are not protected by said gate electrode;

(e) oxidizing an entire remaining portion of said single-crystal Ge comprising layer not protected by said gate electrode, and a less than whole portion of said single-crystal Ge comprising layer under said gate electrode to form a single-crystal Ge comprising island under said single-crystal silicon island and having a first dielectric layer on a first side and a second dielectric layer on second and opposite side of said single-crystal Ge comprising island, said first dielectric layer and said second dielectric layer each extending under said gate electrode; and

(f) forming a polysilicon source region over said first dielectric layer and forming a polysilicon drain region over said second dielectric layer, said polysilicon source region and said polysilicon drain region abutting opposite sides of said single-crystal silicon channel island.

[Claim 21] 21. The method of claim 20, further including, between steps (e) and (f), growing a single-crystal silicon layer on exposed sidewalls of said single-crystal silicon island.

[Claim 22] 22. The method of claim 20, wherein said first dielectric layer extends under a first side of said gate electrode and said second dielectric layer extends under a second and opposite side said gate electrode.

[Claim 23] 23. The method of claim 20, wherein said first dielectric layer extends under a first side of said single-crystal silicon island and said second

dielectric layer extends under a second and opposite side of said single-crystal silicon island.

[Claim 24] 24. The method of claim 20, wherein said first dielectric layer extends under said polysilicon source and said second dielectric layer extends under said polysilicon drain.

[Claim 25] 25. The method of claim 20, wherein:

a first region under said single-crystal silicon island of said first dielectric layer is thicker than a second region of said first dielectric layer under said polysilicon source region; and
a first region under said single-crystal silicon island of said second said dielectric layer is thicker than a second region of said second dielectric layer under said polysilicon drain region.

[Claim 26] 26. The method of claim 20, further including:

forming a single-crystal silicon source region in said single-crystal silicon island, said single-crystal silicon source region abutting said polysilicon source region, said single-crystal silicon source region extending under said gate electrode; and
forming a single-crystal silicon drain region in said single-crystal silicon island, said single-crystal silicon source region abutting said polysilicon drain region, said single-crystal silicon drain region extending under said gate electrode.

[Claim 27] 27. The method of claim 26, wherein:

a first region of said first dielectric layer under said single-crystal silicon channel region has a first thickness and a second region of said first dielectric layer under said polysilicon source region has a second thickness, said first thickness greater than said second thickness;

a first region of said second dielectric layer under said single-crystal silicon channel region has a first thickness and a second region of said second dielectric layer under said polysilicon drain region has a second thickness, said first thickness greater than said second thickness;

said single-crystal silicon source region extends into said polysilicon source region past said first region of said first dielectric layer; and

said single-crystal silicon drain region extends into said polysilicon drain region past said first region of said second dielectric layer.

[Claim 28] 28. The method of claim 26, wherein:

said single-crystal silicon source region does not extend into said single-crystal silicon island past said first region of said first dielectric layer; and

said single-crystal silicon drain region does not extend into said single-crystal silicon island past said first region of said second dielectric layer.

[Claim 29] 29. The method of claim 20, wherein bottom surfaces of said first and second dielectric layers extend into said single-crystal silicon substrate past a bottom surface of said Ge comprising island.

[Claim 30] 30. The method of claim 20, wherein said Ge comprising layer comprises $Si_{(1-X)}Ge_X$ where X equals about 0.15 to about 0.5 or $Si_{(1-X-Y)}Ge_XC_Y$ where X equals about 0.15 to about 0.5 and Y equals about 0 to about 0.1.

[Claim 31] 31. The method of claim 20, wherein said first and second dielectric layers induce stress in the crystal lattice of said single-crystal silicon island.

[Claim 32] 32. The method of claim 20, further including:

doping said single-crystal silicon layer N-type; and

doping said polysilicon source region and said polysilicon drain region drain P-type.

[Claim 33] 33. The method of claim 33, further including:

between steps (e) and (f):

removing said first and second dielectric layers from over said single crystal silicon substrate where said first and second dielectric layers do not extend under said gate electrode or under spacers formed on sidewalls of said gate electrode;

removing a layer of said single crystal silicon substrate from under remaining first and second dielectric layers; and

growing a first single-crystal silicon layer on exposed sidewalls of said single-crystal silicon island and a second single crystal layer on exposed surfaces of said single crystal silicon substrate.

[Claim 34] 34. The method of claim 33, wherein said first dielectric layer extends under a first side of said gate electrode and said second dielectric layer extends under a second and opposite side said gate electrode.

[Claim 35] 35. The method of claim 33, wherein said first dielectric layer extends under a first side of said single-crystal silicon island and said second dielectric layer extends under a second and opposite side of said single-crystal silicon island.

[Claim 36] 36. The method of claim 33, wherein said first dielectric layer does extend under said polysilicon source and said second dielectric layer does not extend under said polysilicon drain.

[Claim 37] 37. The method of claim 33, further including:

forming a single-crystal silicon source region in said single-crystal silicon island, said single-crystal silicon source region abutting said polysilicon source region, said single-crystal silicon source region extending under said gate electrode; and

forming a single-crystal silicon drain region in said single-crystal silicon island, said single-crystal silicon source region abutting said polysilicon drain region, said single-crystal silicon drain region extending under said gate electrode.

[Claim 38] 38. The method of claim 37, wherein:

said single-crystal silicon source region extends into said polysilicon source region past said first dielectric layer; and

said single-crystal silicon drain region extends into said polysilicon drain region past said second dielectric layer.

[Claim 39] 39. The method of claim 37, wherein:

said single-crystal silicon source region does not extend into said single-crystal silicon island past said first region of said first dielectric layer; and

said single-crystal silicon drain region does not extend into said single-crystal silicon island past said first region of said second dielectric layer.

[Claim 40] 40. The method of claim 33 wherein bottom surfaces of said first and second dielectric layers extend into said single-crystal silicon substrate past a bottom surface of said Ge comprising island.

[Claim 41] 41. The method of claim 33, wherein said Ge comprising layer comprises $Si_{(1-X)}Ge_X$ where X equals about 0.15 to about 0.5 or $Si_{(1-X-Y)}Ge_XC_Y$ where X equals about 0.15 to about 0.5 and Y equals about 0 to about 0.1.

[Claim 42] 42. The method of claim 33, wherein said first and second dielectric layers do not induce stress in the crystal lattice of said single-crystal silicon island.

[Claim 43] 43. The method of claim 33, further including:

doping said single-crystal silicon layer P-type; and

doping said polysilicon source region and said polysilicon drain region drain N-type.